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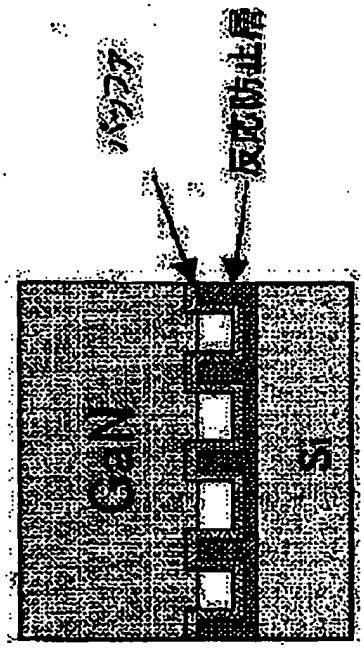
(54) METHOD OF MANUFACTURING SEMICONDUCTOR SUBSTRATE AND SEMICONDUCTOR ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To make a semiconductor single crystal free of cracks, polycrystal lumps, etc., on an Si substrate.
SOLUTION: A reaction-inhibiting layer is formed in order to prevent the reaction of Si and a semiconductor of a gallium nitride system and the reaction-inhibiting layer (crystalline material B) consisting of, for example, SiC or AlN, etc., having a melting point or heat resistance higher than that of the semiconductor (semiconductor crystal A) of the gallium nitride system is deposited on the ground surface substrate (Si substrate) in the manner described above, by which the 'reaction section' consisting of GaN polycrystal lumps, etc., near the silicon boundary is no longer formed even in the case the crystal of the semiconductor (semiconductor crystal A) of the gallium nitride system is grown for a long time. Also, many projecting parts are formed, by which the semiconductor (semiconductor crystal A) of the gallium nitride system is grown in a transverse direction as well with the planar apexes of the projecting parts as start points. As a result, the stress between the antireaction layer and the semiconductor crystal A is drastically relieved and the through-cracks of the longitudinal direction are not produced in the reaction-inhibiting layer and therefore the Si substrate can be surely shut off and the reaction-inhibiting effect is made sure.



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* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] On the ground substrate formed from silicon (Si) using the longitudinal direction crystal-growth operation characterized by providing the following How to obtain a semiconductor substrate by growing up the semiconducting crystal A which consists of an III group nitride system compound semiconductor. The reaction prevention process which forms the reaction prevention layer which consists of the aforementioned semiconducting crystal A on the aforementioned ground substrate from the crystalloid material B with high melting point or thermal resistance. The height formation process which forms many heights from the aforementioned reaction prevention layer, without exposing the aforementioned ground substrate on one side of the side by which the aforementioned reaction prevention layer was formed by chemical or physical etching. The crystal-growth process to which a part of front face [at least] of the aforementioned height is made into the first growth side where the aforementioned semiconducting crystal A starts a crystal growth, and the crystal growth of the aforementioned semiconducting crystal A is carried out until this growth side is connected mutually respectively and it grows up to be a series of abbreviation flat surfaces at least.
[Claim 2] As for the aforementioned semiconducting crystal A, an empirical formula fills "Alx Gay In (1-x-y) N (0<=x<1, 0< y<=1, x+y<=1)". The manufacture method of the semiconducting crystal according to claim 1 characterized by consisting of an III group nitride system compound semiconductor.
[Claim 3] The aforementioned crystalloid material B which forms the aforementioned reaction prevention layer is the manufacture method of the semiconducting crystal according to claim 1 or 2 characterized by consisting of carbonization silicon (SiC), alumimium nitride (AlN), or a spinel (MgAl 2O4).
[Claim 4] The aforementioned crystalloid material B which forms the aforementioned reaction prevention layer is the manufacture method of the semiconducting crystal according to claim 1 or 2 characterized by an aluminum composition ratio consisting of at least 0.30 or more AlGaN(s), AlInN, or AlGaInN.
[Claim 5] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by forming the cavity where the laminating of the aforementioned semiconducting crystal A is not carried out between the aforementioned heights by growing up the aforementioned growth side into a longitudinal direction, and making it connect mutually respectively, or a claim 4.
[Claim 6] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by forming the thickness in the trough of the aforementioned reaction prevention layer between the aforementioned heights in 0.1 micrometers or more and 2 micrometers or less, or a claim 5.

[Claim 7] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by forming the lengthwise height of the aforementioned height in 0.5 micrometers or more and 20 micrometers or less in the aforementioned height formation process, or a claim 6.
[Claim 8] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by forming the size of the longitudinal direction of the aforementioned height, width of face, or a diameter in 0.1 micrometers or more and 10 micrometers or less in the aforementioned height formation process, or a claim 7.
[Claim 9] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by having the partition stage which separates the aforementioned semiconducting crystal A and the aforementioned ground substrate by generating the stress based on the coefficient-of-thermal-expansion difference of the aforementioned semiconducting crystal A and the aforementioned

ground substrate, and fracturing the aforementioned height using this stress by cooling or heating the aforementioned semiconducting crystal A and the aforementioned ground substrate, or a claim 8.
[Claim 10] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by carrying out 50-micrometer or more laminating of the aforementioned semiconductin crystal A in the aforementioned crystal-growth process, or a claim 9.
[Claim 11] It describes above in the aforementioned crystal-growth process. By adjusting the amount of feeding of an III group nitride system compound semiconductor The above in some [at least] corroded fields of the trough between the aforementioned heights of the aforementioned ground substrate The rate of crystal growth a of an III group nitride system compound semiconductor The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by controlling difference (b-a) with the rate of crystal growth b in the parietal region of the aforementione height to abbreviation maximum, or a claim 10.
[Claim 12] They are 1micromol / min about the aforementioned amount q of feeding. They are 100micromol / min above. The manufacture method of the semiconducting crystal according to claim 1 characterized by setting it as below.
[Claim 13] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by having the process which forms in the front face of the aforementioned height at leas buffer-layer C which consists of "Alx Ga1-x N (0< x<=1)" after the aforementioned height formation process, or a claim 12.
[Claim 14] The manufacture method of the semiconducting crystal according to claim 13 characterized by forming the thickness of the aforementioned buffer-layer C in 0.1 micrometers or more and 1 micrometer or less.
[Claim 15] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by forming the aforementioned height in the aforementioned height formation process so that the aforementioned height may be arranged abbreviation regular intervals or an abbreviation fixed period, or a claim 14.
[Claim 16] The manufacture method of the semiconducting crystal according to claim 15 characterized by forming the aforementioned height in the aforementioned height formation process on the lattice point of the two-dimensional triangular grid to which one side makes the keynote the abbreviation equilateral triangle of 0.1 micrometers or more.
[Claim 17] It is the manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by the horizontal section configuration of the aforementioned height being an abbreviatior equilateral triangle, an approximate regular hexagon, an approximate circle form, an abbreviation rectangle, an abbreviation rhombus, or an abbreviation parallelogram in the aforementioned height formation process, or a claim 16.
[Claim 18] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by forming the arrangement interval of the aforementioned height in 0.1 micrometers or more and 10 micrometers or less in the aforementioned height formation process, or a claim 17.
[Claim 19] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by forming the aforementioned reaction prevention layer to front reverse side both sides on the aforementioned ground substrate in the aforementioned reaction prevention process, or a claim 18.
[Claim 20] It is characterized by having the aforementioned semiconducting crystal manufactured by any 1 term of a claim 1 or a claim 19 using the manufacture method of the semiconducting crystal a publication as a crystal-growth substrate. III group nitride system compound semiconductor element.
[Claim 21] It is characterized by what was manufactured by the crystal growth which used as the crystal-growth substrate the aforementioned semiconducting crystal manufactured by any 1 term of a claim 1 or a claim 19 using the manufacture method of the semiconducting crystal a publication. III group nitride system compound semiconductor element.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention is on the ground substrate formed from silicon (Si). By growing up the crystal which consists of an III group nitride system compound semiconductor, it is related with the method of obtaining a semiconductor substrate. Moreover, this invention is manufactured considering such a semiconductor substrate as a crystal-growth substrate. I is related with III group nitride system compound semiconductor element.
[0002]
[Description of the Prior Art] The typical cross section of the conventional semiconducting crystal which carried out the crystal growth to drawing 5 on Si substrate (ground substrate) is illustrated. The MOCVD method was adopted as this crystal-growth process. in the semiconducting crystals (GaN crystal etc.) which are illustrated to this drawing 5 and which carried out elevated-temperature growth on Si substrate (ground substrate) by the Prior art, the "reaction section", transposition, a crack, etc. have arisen like
[0003]
[Problem(s) to be Solved by the Invention] Transposition and a crack cause degradation of a device property, when it is generated as a result of the operation of stress generated based on the coefficient-of-thermal-expansion difference and lattice constant difference between dissimilar materials and various kinds of semiconductor devices by such crystal-growth substrate are manufactured. Moreover, when the ground substrate which consists, for example of silicon (Si) etc. tends to be removed, it is going to leave only a growth phase and it is going to obtain the independent substrate (crystal), it is almost impossible to obtain the thing of a large area (more than 1cm2) by operation of the above-mentioned transposition, a crack, etc.
[0004] Moreover, near 1000 degrees C - 1150 degree C which is the crystal-growth temperature of the target semiconductor substrate (semiconducting crystal A), silicon (Si) and a gallium nitride (GaN) may react and GaN ("reaction section" in drawing) of a polycrystal may be formed. For this reason, there is a problem without easy obtaining the GaN substrate of a single crystal through a hot crystal-growth process.
[0005] Accomplishing this invention in order to solve the above-mentioned technical problem, the purpose is obtaining a quality semiconducting crystal without a crack or a polycrystal lump (reaction section), using comparatively cheap silicon (Si) as a ground substrate. Moreover, the further purpose of this invention is manufacturing a quality semiconductor device by using the above-mentioned semiconducting crystal manufactured with high quality as a crystal-growth substrate.
[0006]
[A The means for solving a technical problem, an operation, and an effect of the invention] The following meanses are effective in order to solve the above-mentioned technical problem. That is, the 1st means is on the ground substrate formed from silicon (Si) using a longitudinal direction crystal-growth operation. In the manufacturing process of a semiconductor substrate into which the semiconducting crystal A which consists of an III group nitride system compound semiconductor is grown up By the reaction prevention process which forms the reaction prevention layer which consists of the crystalloid material B with high melting point or thermal resistance from a semiconducting crystal A on a ground substrate, and chemical or physical etching The height formation process which forms many heights from this reaction prevention layer, without exposing a ground substrate on one side of the side by which the reaction prevention layer was formed, It is establishing the crystal-growth process to which

the crystal growth of the semiconducting crystal A is carried out until it makes a part of front face [at least] of this height into the first growth side where a semiconducting crystal A starts a crystal growth this growth side is connected mutually respectively and it grows up to be a series of abbreviation flat surfaces at least.

[0007] However, even if the above-mentioned semiconductor substrate which consists of above-mentioned semiconducting crystals A is monolayer structure, it may be a double layer structure (multilayer structure). moreover, to general "III group nitride system compound semiconductor" said here The semiconductor of the arbitrary mixed-crystal ratios expressed with 2 yuan, 3 yuan, or 4 yuan the general formula which "Alx Gay In (1-x-y) N (0<=x<=1, 0<=y<=1, 0 <=x+y<=1) N" Changes is contained. Furthermore, also let the semiconductor with which p type or the n type impurity was added be the criteria of the "III group nitride system compound semiconductor" of this specification. Moreover, the above Let the semiconductor which replaced the part of the III group elements (aluminum, Ga, In) with boron (B), the thallium (Tl), etc., or replaced some nitrogen (N) by Lynn (P), arsenic (As), antimony (Sb), the bismuth (Bi), etc. be the criteria of the "III group nitride system compound semiconductor" of this specification.

[0008] moreover — as the impurity of the above-mentioned p type — magnesium (Mg) — or calcium (calcium) etc. can be added Moreover, as an impurity of the above-mentioned n type, silicon (Si), sulfur (S), a selenium (Se), a tellurium (Te) or germanium (germanium), etc. can be added, for example. Moreover, these impurities may add two or more elements simultaneously, and may add both molds (p type and n type) simultaneously.

[0009] Drawing 1 is a typical cross section in the manufacturing process of the semiconducting crystal which explains the fundamental concept of this invention in instantiation. This reaction prevention layer is for preventing the reaction of Si and the semiconductor of a gallium-nitride system. Thus, by forming the reaction prevention layer (crystalloid material B) with the melting point or thermal resistance higher than the semiconductor (semiconducting crystal A) of a gallium-nitride system which consists, for example of SiC, AlN, etc. on a ground substrate (Si substrate) When carrying out the crystal growth of the semiconductor (semiconducting crystal A) of a gallium-nitride system for a long time, it is lost that the aforementioned "reaction section" is formed near a silicon interface.

[0010] Moreover, the semiconductor (semiconducting crystal A) of a gallium-nitride system grows up to be also a longitudinal direction with the common crowning of a height as the starting point by forming many heights. Thereby, it is hard coming to generate the stress based on the lattice constant difference between a reaction prevention layer and the semiconducting crystal A of a gallium-nitride system, and stress is eased sharply.

[0011] Moreover, by forming many heights, it is hard coming to work like and, therefore, the crack which forms a lengthwise crack in a reaction prevention layer and which was penetrated to lengthwise stops easily easing the stress which acts on a reaction prevention layer, and being able to generate such stress in a reaction prevention layer. For this reason, in a reaction prevention layer without the crack penetrated to lengthwise, since a ground substrate (Si substrate) and the semiconductor (semiconducting crystal A) of a gallium-nitride system can be intercepted completely, generating of the above "reaction sections" can be prevented more certainly.

[0012] Moreover, since the contact part of a reaction prevention layer and a semiconductor substrate (namely, the desired semiconducting-crystal layer A) is narrowly limited by, for example, forming the above heights, the distortion based on both lattice constant difference cannot become large easily, and "the stress based on the lattice constant difference between a ground substrate and a semiconductor substrate" is eased. For this reason, in case a semiconductor substrate (the desired semiconducting crystal A) carries out a crystal growth, the unnecessary stress committed to the semiconductor substrate under growth is suppressed, and the generating density of dislocation or a crack is reduced. namely, the above stress relaxation operation — the semiconductor (semiconducting crystal A) of a gallium-nitride system — dislocation — generating — being hard — moreover, the generating density of a crack is also boiled markedly and can be cut down

[0013] It becomes possible [obtaining the quality semiconductor substrate (semiconducting crystal A) without "the above-mentioned reaction section" and an above-mentioned crack by which dislocation density was suppressed enough according to the above operation and the synergistic effect], or easy.

[0014] In addition, when buffer-layer C in this view should just take the form inserted if needed and this invention is carried out, such a buffer layer is not the component which is not necessarily needed. That is, when not preparing a buffer layer, it is possible to acquire an operation and effect of this invention more than fixed.

[0015] Moreover, in the 1st means of the above [the 2nd means], an empirical formula fills "Alx Gay I (1-x-y) N (0<=x<1, 0< y<=1, x+y<=1)" for the above-mentioned semiconducting crystal A. It is constituting from an III group nitride system compound semiconductor.
[0016] Moreover, the 3rd means is using carbonization silicon (SiC), alumimium nitride (AlN), or a spine (MgAl 2O4) in the above 1st or the 2nd means as a crystalloid material B which forms a reaction prevention layer.
[0017] Moreover, the 4th means is that an aluminum composition ratio uses at least 0.30 or more AlGa (s), AlInN, or AlGaInN in the above 1st or the 2nd means as a crystalloid material B which forms a reaction prevention layer. Furthermore, as a crystalloid material B, it is desirable for a lattice constant to choose a comparatively firm heat-resistant (melting point) stable high material of a less than 3.18A interatomic bonding force.
[0018] Moreover, the 5th means is that a semiconducting crystal A forms between heights the cavity b which a laminating is not carried out in any the above 1st or 4th one means by growing up a growth sid into a longitudinal direction, and making it connect mutually respectively. Since the growth side of an abbreviation plane may become is hard to be acquired after connection if too not much large although such a cavity is so desirable that it is made greatly, cautions are required. Moreover, if too small, since the stress relaxation operation by longitudinal direction growth will also become small, cautions are required.
[0019] Moreover, the 6th means is forming the thickness in the trough of the reaction prevention layer between heights in 0.1 micrometers or more and 2 micrometers or less in any the above 1st or 5th one means.
[0020] If this thickness is too thin, since nonuniformity will follow on thickness, or since the above-mentioned crystalloid material B which forms a reaction prevention layer is not the matter stable enough, it becomes impossible to intercept completely a gallium (Ga) or a gallium nitride (GaN), and silicon (Si). Therefore, the effect of preventing formation of "the reaction section (GaN of a polycrystal)" based on these reactions is no longer acquired fully.
[0021] When the thickness in the trough of a reaction prevention layer is too thick, a crack becomes easy to go into the trough of a reaction prevention layer, and it becomes impossible moreover, to intercept completely a gallium (Ga) or a gallium nitride (GaN), and silicon (Si). Therefore, the effect of preventing formation of the "reaction section" based on these reactions is no longer acquired fully. Moreover, if the thickness in the trough of a reaction prevention layer is too thick, since only the part is too many needed, it is not desirable in respect of a production cost etc. [of the laminating time or the charge of plywood of a reaction prevention layer]
[0022] Moreover, the 7th means is forming the lengthwise height of a height in 0.5 micrometers or more and 20 micrometers or less in the height formation process of any the above 1st or 6th one means. The lengthwise height of a height has 1 micrometers or more and good 5 micrometers or less more desirably

[0023] It becomes [the aforementioned cavity becomes small, or it becomes inadequate longitudinal direction growing up / of a semiconducting crystal A / it, and / stress relaxation acting] inadequate an is not desirable if this height is too low. Moreover, if this height is too high, since only the part is too many needed, it is not desirable in respect of a production cost etc. [of laminating time, etching time, o a charge of plywood of a reaction prevention layer]
[0024] Moreover, the 8th means is forming the size of the longitudinal direction of a height, width of face, or a diameter in 0.1 micrometers or more and 10 micrometers or less in the height formation process of any the above 1st or 7th one means. More desirably, although it is dependent also on the operation conditions of a crystal growth, the size of the longitudinal direction of a height, width of face, or a diameter has good about 0.5-5 micrometers.
[0025] If this size is too thick, the influence of stress which works to a semiconductor substrate (growth phase) based on a lattice constant difference will become large, and it will become easy to increase the number of dislocation of a semiconductor substrate. Moreover, if too thin, the own formation of a height becomes difficult, or the rate of crystal growth b of the parietal region of a height becomes slow, and it is not desirable.
[0026] Moreover, the 9th means is preparing the partition stage which separates a semiconducting crystal A and a ground substrate by generating the stress based on the coefficient-of-thermal-expansion difference of a semiconducting crystal A and a ground substrate, and fracturing a height using this stress by setting for any the above 1st or 8th one means, and cooling or heating a semiconducting crystal A and a ground substrate.

[0027] For example, on the ground substrate which has many heights so that it may illustrate to drawi 1 When growing up the semiconductor substrate (semiconducting crystal A) which consists of an III group nitride system compound, a semiconducting crystal A can form the "cavity" by which a laminati is not carried out between each height (side of a height) by adjusting the size and arrangement interva of a height, crystal-growth terms and conditions, etc. For this reason, if a semiconductor substrate (semiconducting crystal A) is made thick enough as compared with the height of a height, internal stre or external stress will become easy to act on this height intensively. When it acts as shearing stress t a height etc. and this stress becomes large, a height fractures the result, especially such stress. Therefore, if this stress is used, it will become possible to separate a ground substrate and a semiconductor substrate easily (exfoliation). Moreover, it becomes easy to concentrate stress (shearir stress) on a height, so that the above-mentioned "cavity" is formed greatly. That is, according to the 9th above-mentioned means, since the above-mentioned stress is easily generable, a semiconducting crystal A and a ground substrate are easily separable.

[0028] In addition, in case a ground substrate and a semiconductor substrate are separated (ablation), part of semiconductor substrate may remain in a ground substrate side, or a part of ground substrate (example : fracture wreckage of a height) may remain in a semiconductor substrate side. Namely, the above-mentioned partition stage is not premised on perfect separation of each material which mak s some wreckage of such material there be nothing (requirement). Removal of such fracture wreckage et can also be carried out using the means of common knowledge, such as wrapping and etching, if neede

[0029] Moreover, the 10th means is carrying out 50-micrometer or more laminating of the semiconducting crystal A in the above 1st or the crystal-growth process of any 9th one means. Since the tensile stress to a semiconductor substrate (semiconducting crystal A) is eased, the generating density of the transposition of a semiconductor substrate or a crack can be decreased and a semiconductor substrate can be simultaneously strengthened so that this thickness is thick, it become that it is easy to centralize the above-mentioned stress on the above-mentioned height.

[0030] Moreover, the thickness of a ground substrate (Si substrate) has desirable 300 micrometers or less. The tensile stress to a semiconductor substrate (semiconducting crystal A) is eased, and the generating density of the transposition of a semiconductor substrate or a crack decreases, so that this thickness is thin. However, if thickness of a ground substrate is set to less than 50 micrometers, a problem will arise about own absolute intensity of a ground substrate, and it will become difficult to maintain high productivity. Therefore, in order to secure the quality and the productivity of a crystal-growth substrate to manufacture, the thickness of a ground substrate has 50 micrometers or more desirable 300 micrometers or less.

[0031] moreover, the thickness of the semiconductor substrate (semiconducting crystal A) which carries out a crystal growth relatively — the thickness of a ground substrate (Si substrate), and abbreviation — it is desirable to suppose that it is equivalent or to carry out to more than it Th tensil stress to a semiconductor substrate becomes that it tended to ease such a setup, and it becomes possible to suppress the transposition of a semiconductor substrate, and generating of a crack more sharply than before. This effect becomes so large that a semiconductor substrate is thickened relatively.

[0032] moreover, the 11th means is set at the above 1st or the crystal-growth process of any 10th one means — it can set to some [at least] corroded fields of the trough between the heights of a ground substrate by adjusting the amount q of feeding of an III group nitride system compound semiconductor is controlling the difference (b-a) of the rate of crystal growth a of an III group nitride system compoun semiconductor, and the rate of crystal growth b in the parietal region of a height to abbreviation maximum.

[0033] According to this means, the rate of crystal growth near the parietal region of a height becomes large relatively, and the crystal growth near [above] a corroded field is suppressed comparatively, and becomes dominant [the crystal growth from near the parietal region]. Consequently, longitudinal direction growth of the semiconductor substrate (semiconducting crystal A) started from near the parietal region of a height becomes remarkable, and "the stress based on the lattice constant differenc between a reaction prevention layer and a semiconductor substrate" committed to a semiconductor substrate at the time of the crystal growth of a semiconductor substrate is eased. Therefore, the crystal structure of a semiconductor substrate is stabilized and it is hard coming to generate transposition and a crack in a semiconductor substrate. Moreover, if longitudinal direction growth (ELO) of a semiconductor substrate becomes remarkable, a comparatively big cavity will become easy to be

made in the side (between each height) of a height, for example.
[0034] When irregularity is formed on the front face of a ground substrate a suitable size, an interval, c a period, generally except the periphery part near the periphery side attachment wall of a ground substrate, the direction of the amount of supply per the unit time and unit area of crystal material of a crevice (trough) tends to decrease compared with near the upper surface of heights (height). This inclination becomes possible [controlling the above-mentioned difference (b-a) to abbreviation maximum] by controlling these terms and conditions the optimal or suitably, although it depends in the flow rate of the gas stream of crystal material, temperature, the direction, etc.
[0035] Moreover, it sets for the 11th above-mentioned means, and the 12th means is 1micromol / min about the amount q of feeding. They are 100micromol / min above. It is setting it as below.
[0036] The more desirable above-mentioned amount q of feeding is 5micromol / min. They are 90micromol / min above. The following is good. Furthermore, although it depends also on terms and conditions, such as specification of ground substrates, such as a size of the height formed, and a form, an arrangement interval, a kind of feed, and the direction of feeder current, a crystal-growth method, a a desirable value, they are 10-80micromol / min in general. A grade is ideal. Since it will become difficu to control the above-mentioned difference (b-a) to abbreviation maximum if this value is too large, it becomes difficult to form a big cavity between each height (side of a height). As for the crystallinity of the single crystal of a semiconductor substrate, it becomes easy to deteriorate and is not desirable to follow, in such a case for the stress in the crystal based on a lattice constant difference comparatively to be hard to be eased, and for dislocation to occur etc.
[0037] moreover, the time of stress (shearing stress) separating a ground substrate and a semiconductor substrate — a height — if there is no cavity of the side or this cavity is small — a height — stress — concentrating — being hard — fracture of a height is hard coming to happen and is not desirable On the other hand, if the amount q of feeding is too small, crystal-growth time will be taken too much and it will become disadvantageous in respect of productivity, and it is not desirable.
[0038] Moreover, the 13th means is establishing the process which forms buffer-layer C which consists of "Alx Ga1-x N (0< x<=1)" on the surface of a height at least after a height formation process in any the above 1st or 12th one means.
[0039] However, the above-mentioned buffer-layer C is semiconductor layers which grow near 400 degrees C - 1100 degree C, such as AlN and AlGaN. Buffer-layer C of another further the above [C / buffer-layer / this], and the interlayer of **** composition (example : AlN and AlGaN) (it may only be hereafter called a "buffer layer") other periodic or layers and alternation -- or you may carry out a laminating into a semiconductor substrate (semiconducting crystal A) so that multilayer structure may be constituted
[0040] The same operation principle as the former of being able to ease the stress committed to the semiconductor substrate (growth phase) resulting from a lattice constant difference by the laminating o these buffer layers (or interlayer) enables it to raise crystallinity. Moreover, in the case of carbonization silicon (SiC) etc., such an operation and an effect have the especially remarkable crystalloid material B which constitutes a reaction prevention layer.
[0041] Moreover, the 14th means is forming the thickness of buffer-layer C in 0.01 micrometers or mor and 1 micrometer or less in the 13th above-mentioned means.
[0042] By this means, the semiconducting crystal A of the request formed on a buffer layer (example : GaN layer) can be grown up into a longitudinal direction good.
[0043] In addition, the thickness of a buffer layer has 0.1 micrometers or more and good 0.5 micrometers or less more desirably, although about 0.01 micrometers - about 1 micrometer is as above mentioned a in general appropriate range. A cavity becomes easy to become small and is not desirable i this thickness is too thick. Moreover, if this thickness is made thin too much, it will become difficult to form a buffer layer to abbreviation homogeneity. If the membrane formation nonuniformity (part which is not fully formed) of a buffer layer arises in near the upper part of a height especially, it becomes easy t produce nonuniformity also in crystallinity, and is not desirable.
[0044] Moreover, the 15th means is forming a height so that a height's may be arranged abbreviation regular intervals or an abbreviation fixed period in the height formation process of any the above 1st or 14th one means.
[0045] Thereby, it becomes equal on the whole omitting the growth conditions of longitudinal direction growth, and it is hard coming to generate nonuniformity in a crystalline quality. Moreover, by this means since the above-mentioned cavity serves as a size with an equal abbreviation respectively and becomes possible [distributing the above-mentioned shearing stress to each height equally / abbreviation],

fracture of all heights arises without nonuniformity and separation with a ground substrate and a semiconductor substrate can carry out certainly. moreover, the crystal-growth method the late crystal growth method of the rate of crystal growth to the rate of crystal growth is quick since it is hard comi to generate local variation at time until the upper part of the trough between heights is completely covered by the semiconductor substrate — on the way — the case where come out and a crystal-growth method is changed — the time — exact — an early stage — or it becomes easy it to be decided for that it will be a meaning

[0046] Moreover, the 16th means is forming a height on the lattice point of the two-dimensional triangular grid to which one side's makes the keynote the abbreviation equilateral triangle of 0.1 micrometers or more in the height formation process of the 15th above-mentioned means.

[0047] By this means, the 15th above-mentioned means can be carried out correctly and certainly mor concretely, and, therefore, the number of dislocation can be reduced certainly.

[0048] Moreover, the 17th means is making the horizontal section configuration of a height into an abbreviation equilateral triangle, an approximate regular hexagon, an approximate circle form, an abbreviation rectangle, an abbreviation rhombus, or an abbreviation parallelogram in the height formatio process of any the above 1st or 16th one means.

[0049] the direction of the crystallographic axis of the crystal formed from an III group nitride system compound semiconductor of this means — each part — a set — easy — arbitrary horizontal direction since it becomes — receiving — length with a horizontal height (size) — abbreviation — since it can restrict uniformly, the number of dislocation can be suppressed Since a right hexagon, an equilateral triangle, a parallelogram, etc. especially tend to agree with the crystal structure of a semiconducting crystal, it is more desirable. Moreover, a round shape and a rectangle have the merit compared with the present condition of the present general processing technical level referred to as being easy to form in respect of a manufacturing technology.

[0050] Moreover, the 18th means is forming the arrangement interval of a height in 0.1 micrometers or more and 10 micrometers or less in the height formation process of any the above 1st or 17th one means. More desirably, although it is dependent also on the operation conditions of a crystal growth, th arrangement interval of a height has good about 0.5-8 micrometers. However, this arrangement interval means the distance between the central point of each height which approaches mutually.

[0051] this means — the upper part of the trough of a height — the target semiconductor substrate (semiconducting crystal A) — a wrap — while things become possible, it becomes possible to form a cavity between heights (trough of a height) If this value is too small, an operation of ELO will no longer be obtained hardly, and a stress relaxation operation cannot fully be obtained, but crystallinity will deteriorate. Unless the cavity formed becomes small too much and makes thickness of a semiconducto substrate larger than required, it becomes impossible moreover, to fracture a height easily.

[0052] Moreover, if this value becomes large too much, it will become impossible to cover the upper par of the trough of a height by the semiconductor substrate certainly, and a semiconductor substrate (semiconducting crystal A) homogeneous [crystallinity] and good will no longer be obtained. Or if this value is still too larger, the exposed surface of a trough will become vast too much, and an operation of ELO will no longer be obtained hardly, and a cavity will no longer be formed at all.

[0053] Moreover, the 19th means is forming a reaction prevention layer to front reverse side both sides on a ground substrate in the reaction prevention process of any the above 1st or 18th one means. Thereby, the curvature (curve) of the ground substrate (Si substrate) produced after a reaction prevention process can be prevented or eased.

[0054] Moreover, in the 20th means and III group nitride system compound semiconductor element, it is having the semiconducting crystal manufactured by any the above 1st or 19th one means as a crystal-growth substrate. According to this means, it becomes crystallinity is good and more possible [manufacturing III group nitride system compound semiconductor element] than a semiconductor with little internal stress, or easy.

[0055] moreover, crystal growth which used as the crystal-growth substrate the semiconducting crysta which boiled and set the 21st means and was manufactured by any the above 1st or 19th one means It is manufacturing III group nitride system compound semiconductor element. According to this means, it becomes crystallinity is good and more possible [manufacturing III group nitride system compound semiconductor element] than a semiconductor with little internal stress, or easy. The aforementioned technical problem is rationally [effectively or] solvable with the means of the above this invention.

[0056]

[Embodiments of the Invention] You may choose each manufacture conditions as arbitration out of a

degree in carrying out this invention, respectively. Moreover, you may combine each of these manufacture conditions arbitrarily. First, as a method of forming an III group nitride system compound semiconductor layer first, an organic-metal vapor growth (MOCVD or MOVPE) is desirable. However, a molecular-beam vapor growth (MBE), a halide vapor growth (Halide VPE), a liquid phase grown method (LPE), etc. may be used, and each class may be formed by the respectively different growth method.
[0057] Moreover, about a buffer layer, it is desirable to form in the inside of a crystal-growth substrate or a ground substrate from the reason of correcting grid mismatching. III group nitride system compour semiconductor AlxGayIn1-x-yN (0<=x<=1, 0<=y<=1, 0 <=x+y<=1) made to form at low temp rature as these buffer layers when carrying out the laminating of the buffer layer (the aforementioned interlayer) into a semiconductor substrate (semiconducting crystal A) especially — AlxGa1-xN (0<=x<=1) can be used more preferably A monolayer is sufficient as this buffer layer, and it is good also as a multiplex layer which is [composition] different. The formation method of a buffer layer may be formed at 380-420-degree C low temperature, and the range of it is 1000-1180 degrees C conversely, and it may be formed by the MOCVD method. Moreover, the buffer layer which consists of AlN by the reactive spatte method can also be formed using DC magnetron-sputtering equipment by making high grade m tal aluminum and nitrogen gas into raw material.
[0058] The buffer layer of general formula AlxGayIn1-x-yN (0<=x<=1, 0<=y<=1, 0 <=x+y<=1, and a composition ratio are arbitrary) can be formed similarly. Furthermore, a vacuum deposition, the ion plating method, the laser ablation method, and the efficient consumer response method can be used. A: for the buffer layer by the physical vapor deposition, it is desirable to carry out at 200-600 degrees C. is 300-600 degrees C still more desirably, and is 350-450 degrees C still more desirably. When physical vapor depositions, such as these sputtering methods, are used, buffer layer thickness has desirable 100-3000A. Still more desirably, 100-400A is desirable and is 100-300A most desirably.
[0059] There is the method of forming by turns as 600 degrees C or less and 1000 degrees C or more i formation temperature about the layer with the same composition which forms by turns the layer which consists, for example of AlxGa1-xN (0<=x<=1), and a GaN layer as a multiplex layer. Of course, these may be combined and a multiplex layer may carry out the laminating of three or more sorts of III group nitride system compound semiconductor AlxGayIn1-x-yN (0<=x<=1, 0<=y<=1, 0 <=x+y<=1). Generally the buffer coat is amorphous and an interlayer is a single crystal. A buffer coat and an interlayer may b formed a term two or more rounds as one period, and a repeat is good an arbitrary period. Crystallinity becomes good, so that there are many repeats.
[0060] Whether it replaces a part of composition of an III group element with boron (B) and a thallium (Tl) or the III group nitride system compound semiconductor of a buffer layer and the upper layer replaces composition of nitrogen (N) part by Lynn (P), the arsenic (As), antimony (Sb), and the bismuth (Bi), it can apply this invention substantially. Moreover, what doped the grade which cannot display these elements on composition may be used. For example, AlxGa1-xN (0<=x<=1) which is the III group nitride system compound semiconductor which does not have an indium (In) and an arsenic (As) in composition may be compensated for the extended distortion of the crystal by the omission of a nitrogen atom with compressive strain with doping the big indium (In) of an atomic radius from aluminum (aluminum) and a gallium (Ga), and doping the big arsenic (As) of an atomic radius from nitrogen (N), and crystallinity may be
[0061] In this case, since acceptor impurity goes into the position of an III group atom easily, p type crystal can also be obtained by the AZUGU loan. Thus, together with the invention in this application, penetration transposition can also be further lowered to 100 or about 1/1000 by improving crystallinity. In the case of the basal layer in which the buffer layer and the III group nitride system compound semiconductor layer are formed two or more periods, it is still better for each III group nitride system compound semiconductor layer to dope an element with a bigger atomic radius than a main composition element. In addition, when it constitutes as a light emitting device, it is desirable to use the 2 yuan system of an III group nitride system compound semiconductor or a 3 yuan system originally.
[0062] When forming an n type III group nitride system compound semiconductor layer, IV group elements, such as Si, germanium, Se, Te, and C, or VI group element can be added as an n type impurity. Moreover, as a p type impurity, II group elements, such as Zn, Mg, Be, calcium, Sr, and Ba, or IV group element can be added. You may dope plurality or n type impurity, and p type impurity for these in the same layer.
[0063] It is also arbitrary to reduce the transposition of an III group nitride system compound semiconductor layer using longitudinal direction epitaxial growth. Under the present circumstances, the method of the thing using a mask and the thing arbitration which buries a level difference by etching cai

be taken.
[0064] An etching mask can be with oxides, such as polycrystal semiconductors, such as polycrystal silicon and a polycrystal nitride semiconductor, oxidization silicon (SiOx), a silicon nitride (SiNx), titaniu oxide (TiOX), and a zirconium oxide (ZrOX), a nitride, titanium (Ti), refractory metals like a tungsten (W and these multilayers. These membrane formation methods are arbitrary besides vapor growths, such a vacuum evaporationo, a spatter, and CVD.
[0065] Although reactant ion beam etching (RIBE) is desirable in case it etches, the arbitrary etching methods can be used. As what does not form the level difference which has the side perpendicular to a substrate side, the cross section which does not have a base in the pars basilaris ossis occipitalis of a level difference by anisotropic etching may form a V character-like thing.
[0066] Semiconductor devices, such as FET and a light emitting device, can be formed in an III group nitride system compound semiconductor. In the case of a light emitting device, although a luminous layer can consider the thing of gay structure besides multiplex quantum well structure (MQW) and singl quantum well structure (SQW), hetero structure, and double hetero structure, you may form by the pin junction or pn junction.
[0067] Hereafter, this invention is explained based on a concrete example. However, this invention is nc limited to the example shown below.
(The 1st example) The outline of the manufacture procedure of the semiconducting crystal (crystal-growth substrate) in the example of this invention is illustrated hereafter.
[0068] [1] A reaction prevention process book reaction prevention process is a manufacturing process which carries out the laminating of the reaction prevention layer on a ground substrate (Si substrate). At this reaction prevention process, about 1.5 micrometers of reaction prevention layers which consist of carbonization silicon (SiC) are first formed by the vapor growth (MOVPE) on Si (111) substrate. In addition, in order to prevent the curvature of a wafer, you may form a SiC film to front reverse side bot sides.
[0069] [2] Form the height B1 of the shape of an approximate circle pilaster with a diameter [of about 1 micrometer], and a height of about 1 micrometer at intervals of about 2-micrometer arrangement by the dry etching using photo lithography on the reaction prevention layer of the height formation proces above (drawing 2). A height B1 is formed so that the center at the base of a pillar of a height B1 may be arranged on each lattice point of the two-dimensional triangular grid which makes the keynote the abbreviation equilateral triangle whose one side is about 2 micrometers as an array gestalt. However, thickness of a ground substrate is set to about 200 micrometers.
[0070] [3] At a crystal-growth process book crystal-growth process, as shown in drawing 4 , carry out growth process until a crystal-growth side is mutually connected respectively from the upper surface (initial state) of a height B1 and grows up to be a series of abbreviation planes according to an organometallic compound vapor growth (the MOVPE method), and carry out a growth process until it grows up to be the thick film this semiconductor substrate (crystal layer) of whose is about 200 micrometers after that according to a hydride vapor growth (the HVPE method). In addition, at this crystal-growth process, it is ammonia (NH3). Gas, carrier gas (H2, N2), trimethylgallium (Ga3 (CH3)) gas (it is described as "TMG" below), and trimethylaluminum (aluminum3 (CH3)) gas (it is described as "TMA" below) are used.
[0071] (a) Organic washing and acid treatment wash first the ground substrate (drawing 2) in which th above-mentioned height B1 was formed, and equip the susceptor laid in the reaction chamber of crystal-growth equipment, and bake a ground substrate at the temperature of 1100 degrees C, passing H2 to a reaction chamber by the ordinary pressure.
(b) Next, supply H2, NH3, TMG, and TMA on the above-mentioned ground substrate according to the MOVPE method, and form an AlGaN buffer layer (buffer-layer C). The crystal-growth temperature of this AlGaN buffer-layer C is about 1100 degrees C, and thickness is about 0.2 micrometers. (Drawing 3)
[0072] (c) On this AlGaN buffer layer (buffer-layer C), it is H2 and NH3 in a part of semiconductor substrate A, i.e., the GaN layer of about 5 micrometers of thickness. And TMG was supplied and the crystal growth was carried out at the growth temperature of 1075 degrees C. According to this process as shown in drawing 4 , a part of semiconductor substrate (GaN layer A) carries out longitudinal direction growth, and a big cavity is made in the side of a trough B1, i.e., a height. In addition, the TMG speed of supply at this time is 40micromol / min in general. It is a grade and the rate of crystal growth of a GaN layer (semiconducting crystal A) is about about 1 micrometer/Hr.
[0073] (d) According to the hydride vapor growth (the HVPE method), the crystal growth of the above-

mentioned GaN layer (semiconducting crystal A) was further carried out to 200 micrometers after that The rate of crystal growth of the GaN layer in this HVPE method is about about 45 micrometer/Hr.
[0074] [4] Partition stage (a) The wafer which has a ground substrate (Si substrate) is cooled to abbreviation ordinary temperature after the above-mentioned crystal-growth process, passing ammoni. (NH3) gas to the reaction chamber of crystal-growth equipment. What is necessary is just to make the cooling rate at this time into the "-50 degree-C/min—5 degree C/min" grade in general.
[0075] (b) When these were taken out from the reaction chamber of crystal-growth equipment after that, the GaN crystal (semiconducting crystal A) which exfoliated from the ground substrate (Si substrate) was obtained. However, this crystal is a thing [that some / small / wreckage of AlGaN buffer-layer C and the fracture wreckage of a height B1 have remained at the rear face of a GaN lay r (semiconductor substrate)].
[0076] [5] Remove the fracture wreckage of the height B1 which consists of Si which remained in the rear face of a GaN crystal by wrapping processing after the partition stage of the fracture wreckage removal process above. However, you may carry out this fracture wreckage removal process by etchin processing using the mixed liquor which added the nitric acid to fluoric acid.
[0077] By the above manufacture method, the semiconductor substrate (semiconducting crystal A) of the good GaN crystal of the crystallinity of about 200 micrometers of thickness which was very excellent (GaN layer), i.e., the request which became independent of a ground substrate, can b obtained.
[0078] In addition, as a crystalloid material B which forms a reaction prevention layer, the operation anc effect as the above-mentioned example and abbreviation that AlN and Alx Ga1-x N (0.30<=x<=1) are also the same are acquired. Generally carbonization silicon (SiC, 3 C-SiC), alumimium nitride (AlN), a spinel (MgAl 2O4), or an aluminum composition ratio can use at least 0.30 or more AlGaN(s), AlInN, or AlGaInN more as a crystalloid material B which forms a reaction prevention layer.
[0079] Moreover, the semiconducting crystal A which forms the target semiconductor substrate is not limited to a gallium nitride (GaN), and can choose arbitrarily the aforementioned general "III group nitrid system compound semiconductor." Moreover, the target semiconductor substrate (semiconducting crystal A) is good also as what has multilayer structure.
[0080] Moreover, although the height and trough of a ground substrate are constituted from an above-mentioned example by a vertical plane and the level surface as illustrated to drawing 2 , you may form these from arbitrary slant faces, curved surfaces, etc. Therefore, the cross-section configuration of the trough formed on the ground substrate illustrated to drawing 2 (c) may be formed in the form of for example, the abbreviation type for U characters, the abbreviation type for V characters, etc. besides th **** type of an abbreviation rectangle, and, generally these configurations, a size, an interval, arrangement, orientation, etc. are arbitrary.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The typical cross section in the manufacturing process of the semiconducting crystal whicl explains the fundamental concept of this invention in instantiation.
[Drawing 2] The typical perspective diagram (a) of the partial fragment of the ground substrate (Si substrate) concerning the example of this invention, a plan (b), and a cross section (c).
[Drawing 3] The typical perspective diagram (a) of the ground substrate by which buffer-layer C (AlGaN layer) was formed, a plan (b), and a cross section (c).
[Drawing 4] The typical perspective diagram (a) of the ground substrate to which the laminating of the semiconductor substrate (semiconducting crystal A) was carried out, a plan (b), and a cross section (c).
[Drawing 5] The typical cross section which illustrates the conventional semiconducting crystal which carried out the crystal growth on Si substrate (ground substrate).
[Description of Notations]
Si — Silicon substrate (ground substrate)
A — Semiconducting crystal (the target semiconductor substrate)
B — Reaction prevention layer (crystalloid material)
B1 — Height (a part of reaction prevention layer)
C — Buffer layer

[Translation done.]